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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant Vikas K. Agrawal, et al. Docket Number: TI-35282

Serial No.: 10/663,575 Art Unit: 2824

Filed: 09/16/03 Examiner: Van Thu T. Nguyen

For: Cycle Ready Circuit for Self-Clocking Memory Device

CERTIFICATION OF FACSIMILE TRANSMISSION

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FACSIMILE COVER SHEET

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___ NEW APPLICATION	___ EOT
___ DECLARATION	___ NOTICE OF APPEAL
___ ASSIGNMENT	___ APPEAL (# Pages)
___ FORMAL DRAWINGS	___ ISSUE FEE & PUBLICATION FEE (1 Page)
___ INFORMAL DRAWINGS	___ REPLY BRIEF (IN TRIPLICATE) (# Pages)
___ CONTINUATION APP'N	___ ELECTION
___ DIVISIONAL APP'N	

NAME OF INVENTOR(S): Vikas K. Agrawal, et al.	RECEIPT DATE & SERIAL NO.: Serial No.: 10/663,575 Filing Date: 09/16/03
TITLE OF INVENTION: Cycle Ready Circuit for Self-Clocking Memory Device	
TI FILE NO.: TI-35282 / DEPOSIT ACCT. NO.: 20-0668	
FAXED: 5-2-05 DUE: 5-2-05 ATTY/SEC'Y: AKS/kjv	

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PO Box 655474, M/S 3999
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Vikas K. Agrawal, et al. **Art Unit:** 2824
Serial No.: 10/663,575 **Examiner:** Van Thu T. Nguyen
Filed: 09/16/03 **Docket:** TI-35282
For: CYCLE READY CIRCUIT FOR SELF-CLOCKING MEMORY DEVICE

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

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AMENDMENT

In response to the Official Action in this case mailed February 2, 2005, please enter the following: